Analysis of the physical properties of the ZnO/ZnCdO and ZnCdO/ZnO layers on Si (111) substrates before and after annealing

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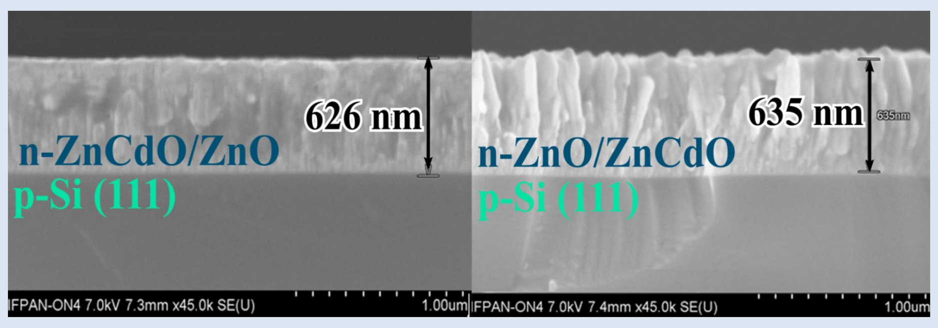
Introduction

Zinc oxide (ZnO), a direct wide band gap (3.37 eV at room temperature) semiconductor has stimulated great research interest due to its unique optical and electrical properties. Cadmium oxide (CdO) is a group of II–VI n-type semiconductor with a room temperature band gap value modulating within the range of ~ 2.18 to 2.31 eV. Alloying of ZnO with CdO leads to the gradual reduction of the bandgap, which results in tuning of luminescence from UV to VIS region. Thus, CdO/ZnO heterostructures can be used in a wide range of light emitting and laser diode sources operating from ultraviolet to green/blue wavelengths.

Samples – basic information

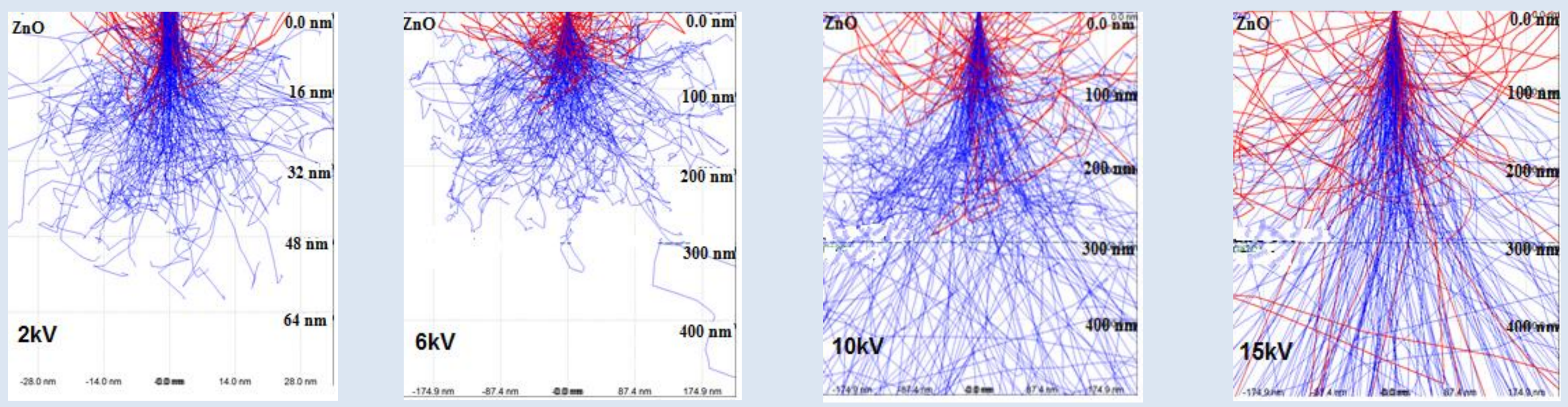
- The films grown by MBE technique
- The growth temperature was of 190°C
- The Cd content in ZnCdO was approximately 1-2%
- Annealing was performer at 700 °C under vacuum
- The ZnO layer was ~400 nm thick, whereas the ZnCdO film was of ~230 nm.

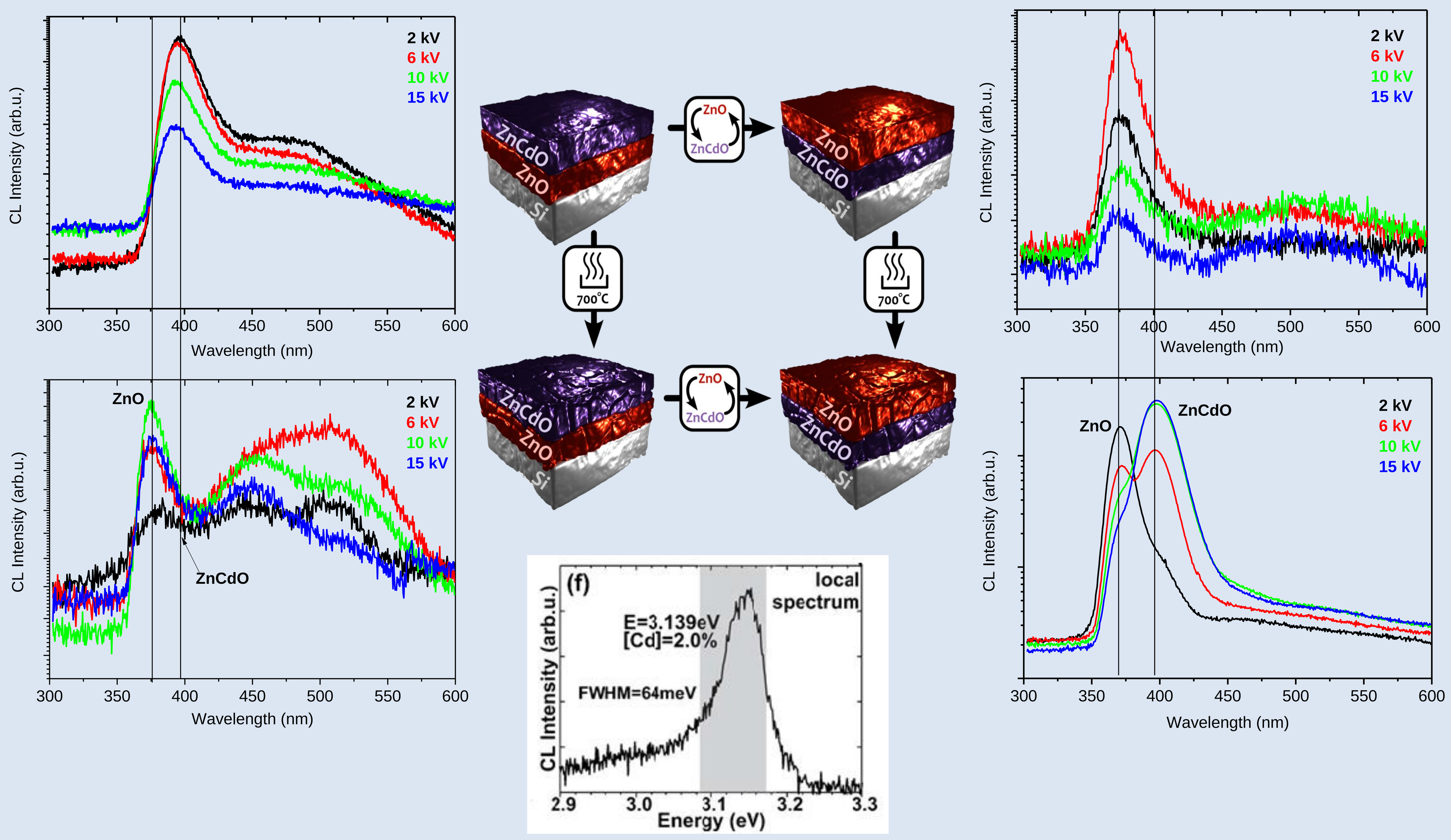


The SEM pictures of heterojunctions [1]

Cathodoluminescence measurements

The excitation profiles for electrons (measured in kV) versus depth obtained for ZnCdO on a Si (111) substrate based on analytic Monte Carlo simulations. The simulations were conducted for 1000 electrons with a beam radius of 3 nm.

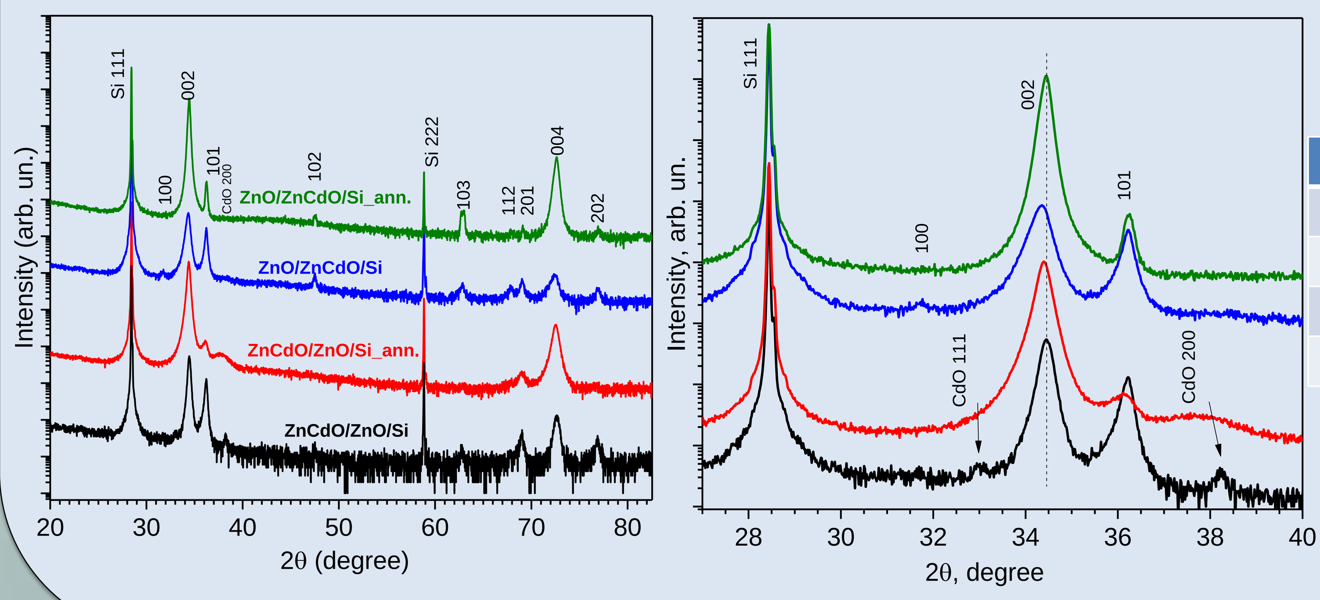




According to Bertram et al., the peak at 3.139 eV (395 nm) corresponds to approximately 2% Cd [2]

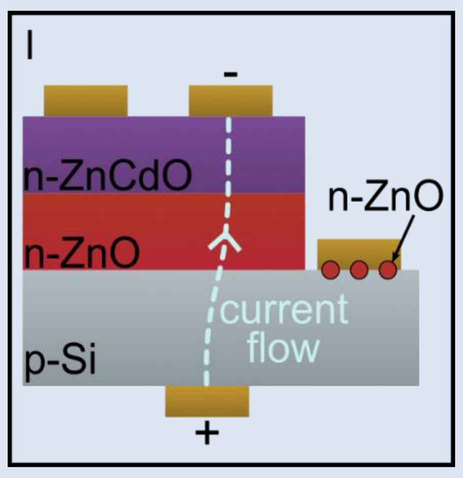
XRD measurements

All the samples have strong diffraction peaks corresponding to (002) facet of ZnO/ZnCdO and ZnCdO/ZnO, indicating that the samples consist mainly of the hexagonal and polar structure. A cubic phase was not registered. After annealing at 700 °C, the peaks intensity increases to some extent, which is likely due to the increasing grain size of the films.

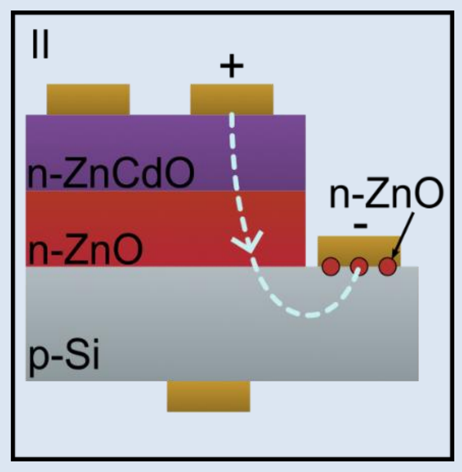


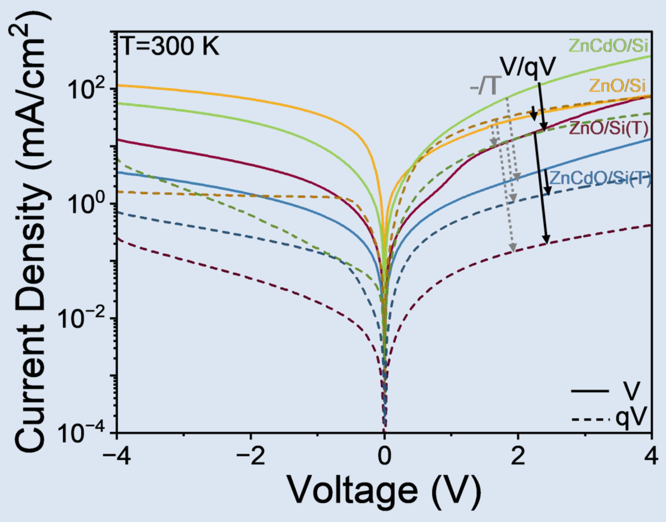
Samples	2θ
ZnCdO/ZnO/Si	34.38
ZnCdO/ZnO/Si annealing	34.49
ZnO/ZnCdO/Si	34.38
ZnO/ZnCdO/Si annealing	34.49

Electrical characteristics

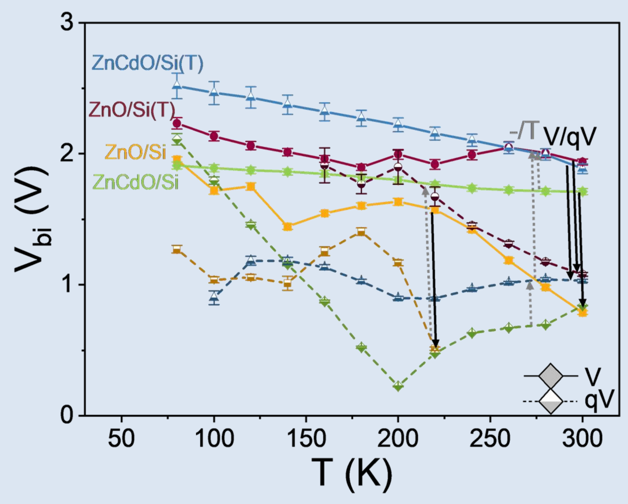


The representative scheme of J-V measurements for ZnO/Si structure in (I) vertical (V) and (II) quasi-vertical (qV) configurations. The current flow, and +/- symbols of polarization were marked for forward bias.

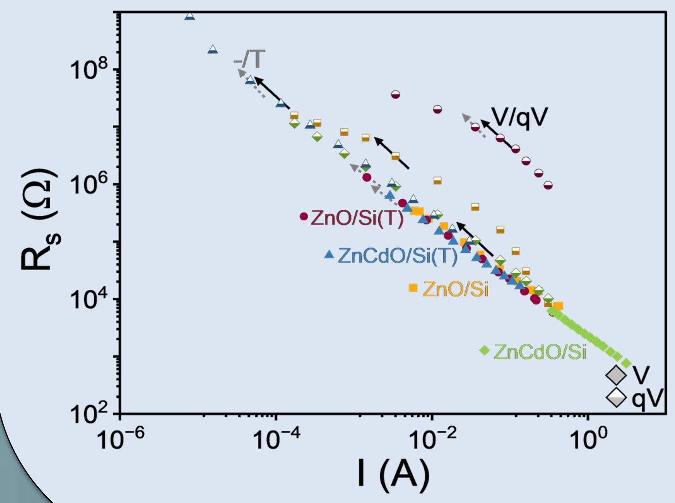




The annealing of the samples lowers the current density in both V and qV configurations.
The qV configuration exhibits worse parameters compared to the V configuration. This is due to the low reverse current density through the n-ZnO/p-Si HJ. The exception is the ZnO/Si sample, for which the reverse and forward current densities were similar.



The built-in potential V_{bi} temperature evolutions show that only in V-configurations, the evolution is regular, whereas in qV-one there is no clear trend, what confirmed its complex composition. The results also show the increase of V_{bi} after HJs annealing, caused probably by increase of surface potential.



Annealing the samples results in higher R_{ser} and lower I(4 V) of the HJs compared to the as-grown layers.
The qV configuration exhibits higher R_{ser} and lower I(4 V), probably due to the dependence on the reverse current flow through the n-ZnO/p-Si HJ.

Summary

- ✓ The ZnO/ZnCdO/Si(111) and ZnCdO/ZnO/Si(111) heterojunctions were successfully grown by MBE technique.
- ✓ XRD measurements indicated that the films were grown along the (002) direction.
- ✓ After annealing at 700 °C in the vacuum, the XRD peaks intensity increased to some extent, which is likely due to the increasing grain size of the films.
- ✓ After annealing, the optical properties of the structures improve. Peaks from ZnO and ZnCdO are visible.
- ✓ The electrical measurements revealed the opportunity for device fabrication in two different configurations.
- ✓ It was shown that the vertical configuration exhibits better performance parameters comapred to the the quasi-verical one, which is affected by the surface and interface states remaining after etching.
- ✓ Annealing of the samples makes the electrical properties worse and especially increases the built-in potential and series resistance, Such effect can be explained by the increase of the surface potential together with the grain size.

[1] R. Szymon et al. J. Alloys Compd. 951 (2023) 169859.
[2] F. Bertram et al. Appl. Phys. Lett. 88 (2006) 061915.

See also:

E. Zielony et al. Appl. Surf. Sci. 538:4 (2021) 148061.
M.A. Pietrzyk et al. Sens. Actuator A Phys. 315 (2020) 112305.